AMENDMENTS TO THE CLAIMS

Claims 1-45 (canceled).

Claim 46 (newly presented) A method for equalizing read latency over a plurality of memory devices at a memory controller of a memory system, the method comprising:

determining a memory system read latency as a maximum of a plurality of minimum device read latencies from said plurality of memory devices; and

for each memory device,

setting said memory device to operate at a device read latency equal to said memory system read latency by adding a latency which is equal to a difference between said memory system read latency and a minimum device read latency of said memory device.

Claim 47 (newly presented) The method of claim 46, wherein said step of determining a memory system ready latency comprises:

sending a command to cause each memory device to output a calibration pattern; and

measuring a number of clock cycles elapsed between said sending a command and a last calibration pattern to be detected.

Claim 48 (newly presented) The method of claim 47, wherein said calibration pattern has at least two successive bits which have different logical states.

Claim 49 (newly presented) The method of claim 48, wherein said calibration pattern comprises a plurality of bits having a first bit set to a first logical state and each subsequent bit set to another logical state.

Claim 50 (newly presented) A method of operating a memory device, comprising:

sending a latency command to said memory device; and

sending a numeric value associated with said latency command to said memory device;

wherein said memory device, in response to said latency command and said numeric value, is set to operate at a device read latency equal a minimum device read latency of said memory plus a number of clock cycles equal to said numeric value.

Claim 51 (newly presented) The method of claim 50, wherein said number is sent over a plurality of configuration lines.

Claim 52 (newly presented) The method of claim 50, further comprising:

at a memory controller,

sending a calibration command to said memory device, said calibration command causing said memory device to output a predetermined calibration pattern; and

measuring a number of clock cycles which elapse between said sending a calibration command and receipt of said predetermined calibration pattern at the memory controller.